JEDEC STANDARD

Serial Flash Reset Signaling Protocol

chengdu

JESD252.01

(Minor editorial revision to JESD252, October 2018)

APRIL 2021

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SERIAL FLASH RESET SIGNALING PROTOCOL

Contents

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Foreword

This standard is intended for use by SoC, ASIC, ASSP, and FPGA developers or vendors interested in incorporating a signaling protocol for hardware resetting the Serial Flash device. In is also intended for use by peripheral developers or vendors interested in providing Serial Flash devices compliant with the standard.

This document was prepared by the JC-42.4_3 Serial Flash task group authorized by the JC-42.4 Non-Volatile Memory subcommittee.

Introduction

This standard defines a signaling protocol that allows the host to reset the targeted Serial Flash device without a dedicated hardware reset pin.

Some Serial Flash devices provide a dedicated RESET# pin that can be used to perform a hardware reset on the device. In such case, when the host asserts RESET# for a specified amount of time, the device will be reset in hardware.

Some Serial Flash devices may not provide such RESET# hardware pin for the function, either due to the size of the package or the pin is shared with an I/O pin by design. In the pin sharing situation, the reset function is disabled if the I/O pin is used in Quad or Octal configuration. Additionally, even if a RESET# hardware pin is available at the Serial Flash device, dedicating a host IO pin for controlling the RESET# signal may not be possible.

This standard specifies a signaling protocol that can be implemented on the Serial Flash interface to perform a hardware reset without a dedicated hardware RESET# pin. If both the host and the device support such protocol, the user can perform a hardware reset function by using only the CS#, SCK, and the SI pins.

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SERIAL FLASH RESET SIGNALING PROTOCOL

(From JEDEC Board Ballot JCB-17-46, formulated under the cognizance of the JC-42.4 Subcommittee on Non-Volatile Memory Devices.)

1 Scope

This standard specifies the signaling protocol for hardware resetting a Serial Flash device. The protocol can be used in the absence of or in addition to a dedicated RESET# pin on the device.

2 Normative Reference

The following normative documents contain provisions that through reference in this text, constitutes provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

JEDEC Manual, JM7.01, *Style Manual for Standards and Other Publications of JEDEC.*

JEDEC Standard, JESD88E, *Dictionary of Terms for Solid-State Technology.*

JEDEC Standard, JESD99C, *Terms, Definitions, and Letter Symbols for Microelectronic Devices.*

JEDEC Standard, JESD100B.01, *Terms, Definitions, and Letter Symbols For Microcomputers, Microprocessors, and Memory Integrated Circuits.*

JEDEC Standard, JESD216, *Serial Flash Discoverable Parameters (SFDP.)*

JEDEC Standard, JESD251, eXpanded Serial Peripheral Interface (xSPI) for Non-Volatile Memory Devices

3 Terms and Definitions

The current version of JESD88, Dictionary of Terms for Solid-State Technology, is the governing document for terms used in this standard. The following terms and definitions are provided for ease of reference:

CS#: Device Chip Select.

IO0: Serial Input and Output zero (some older devices refer to this signal as SI).

IO1: Serial Input and Output one (some older devices refer to this signal as SO).

SCK: Device Serial Clock.

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4 Protocol Description

The Reset Signaling Protocol is shown in Figure 1 and described as follows:

The protocol consists of two phases: reset request, and completion (a device internal reset).

4.1 Reset Request

1. CS# is driven active low to select the SPI target (Note1),
2. Clock (SCK) remains stable in either a high or low state (Note 2),
3. SI / IO0 is driven low by the bus initiator, simultaneously with CS# going active low, (Note 3), and
4. CS# is driven inactive (Note 4).

Repeat the steps 1-4 each time alternating the state of SI (Note 5).

NOTE 1 This powers up the SPI target.

NOTE 2 This prevents any confusion with a command, as no command bits are transferred (clocked).

NOTE 3 No SPI bus target drives SI during CS# low before a transition of SCK, i.e., target streaming output active is not allowed until after the first edge of SCK.

NOTE 4 The target captures the state of SI on the rising edge of CS#.

NOTE 5 SI is low on the first CS#, high on the second, low on the third, high on the fourth (This provides a 5h pattern, to differentiate it from random noise).

4.2 Reset Completion

After the fourth CS# pulse, the target triggers its internal reset.

4.3 Timing Diagram and Timing Parameters

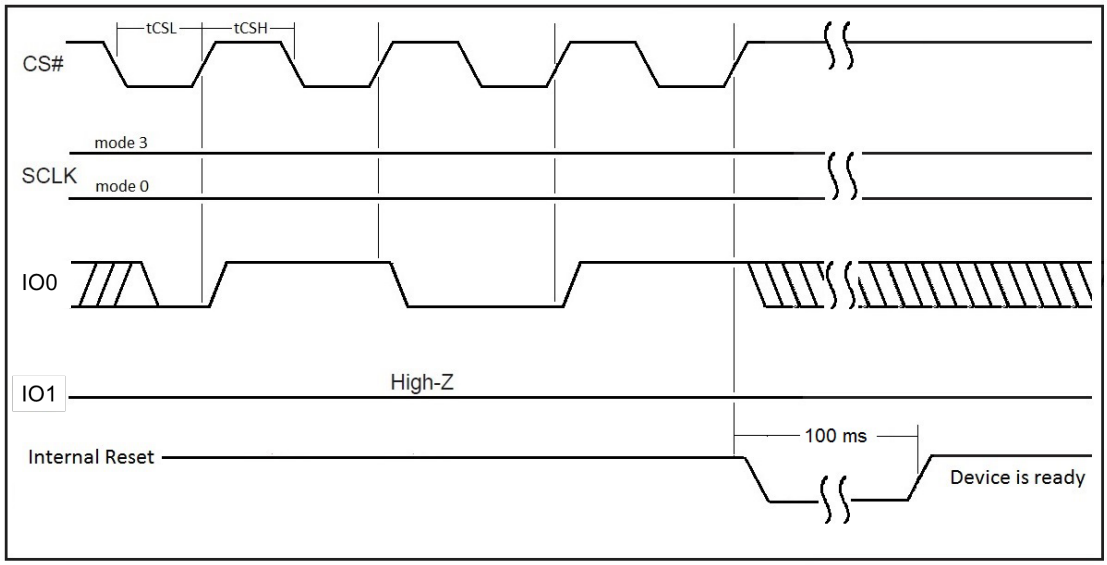

Figure 1 — Reset Signaling Protocol

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4.3 Timing Diagram and Timing Parameters (cont'd)

Table 1 — Timing Parameters

Parameter	Min	Max	Units
tCSL	500	--	ns
tCSH	500	--	ns
Setup Time	5	--	ns
Hold Time	5	--	ns

4.4 Additional Notes and Considerations for the Protocol

NOTE 1 This reset sequence is not intended to be used at normal power up.
NOTE 2 This reset sequence will be operational from any state that the device may be in.
NOTE 3 During the reset process, the device may ignore any commands.

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Annex A (informative) Differences between revisions

This annex briefly describes most of the changes made to entries that appear in this standard, JESD252.01, compared to its predecessor, JESD252 (October 2018). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
3	Removed Term and definition for Si, replaced with term and definition for SCK.

"These changes have been made to comply with the JEDEC Standard Language/Terminology Directive, January 2021.

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